Claims

[c1] 1.A layout of nonvolatile memory, comprising:
a word line;
a bit line;
a plurality of metal-oxide semiconductor (MOS) transistor memory cells, each having a gate electrode, a first doped electrode, and a second doped electrode, wherein each of the first doped electrode is coupled to the bit line, and each of the gate electrode is coupled to a corresponding one of the word line; and
a shared coupled capacitor structure, coupled between the transistor memory cells of the adjacent bit line from the second doped electrodes,
wherein the shared coupled capacitor structure comprises at least two floating-gate MOS capacitors, wherein each of the floating-gate MOS capacitors comprises:
a floating-gate transistor having a floating gate, a first source/drain (S/D) region and a second S/D region; and
a MOS capacitor, coupled to the floating gate,
wherein the first S/D region is coupled to the second doped electrode of the corresponding one of the transistor memory cells, and the second S/D region is shared with an adjacent one of the floating-gate transistor.

[c2] 2. The layout of nonvolatile memory of claim 1, wherein two adjacent bit lines are grouped in a memory group, wherein all of the transistor memory cells between two adjacent bit lines share the same shared coupled capacitor structure

[c3] 3. The layout of nonvolatile memory of claim 2, wherein all of the MOS capacitors are positioned one after one in series.

[c4] 4. The layout of nonvolatile memory of claim 1, wherein the second S/D region is coupled to a first voltage and a substrate end of the MOS capacitor is coupled to a second voltage.

[c5] 5. The layout of nonvolatile memory of claim 1, wherein each of the MOS capacitors comprises two N-type MOS capacitors and one P-type MOS capacitor between the two N-type MOS capacitors in abutting contact.

[c6] 6. A nonvolatile memory cell, comprising:
a metal-oxide semiconductor (MOS) transistor, having a first doped electrode coupled to a bit line, a gate electrode coupled to a word line, and a second doped electrode;
a floating-gate MOS transistor, having a first source/drain (S/D) region coupled to the second doped elec-

trode, a second S/D region coupled to a first voltage terminal, and a floating gate; and

a MOS capacitor, having a gate-capacitor electrode coupled to the floating gate of the floating-gate MOS transistor, and a substrate-capacitor electrode coupled to a second voltage terminal.

[c7] 7. The nonvolatile memory cell of claim 6, wherein when a programming process is operated, the bit line is applied with a ground voltage to select the memory cell, the first voltage terminal and the second voltage terminal are applied with a first voltage, and the word line is applied with a second voltage, so that hot electrons are injected into the floating gate of the floating-gate MOS transistor.

[c8] 8. The nonvolatile memory cell of claim 7, wherein the word line and the bit line of a non-selected memory cell are respectively applied with the ground voltage and a system voltage source.

[c9] 9. The nonvolatile memory cell of claim 6, wherein when a read process is operated, the bit line is applied with an intermediate voltage to select the memory cell, the first voltage terminal is applied with a ground voltage, the second voltage terminal are applied with a first voltage, and the word line is applied with a second voltage.

[c10] 10. The nonvolatile memory cell of claim 9, wherein the word line and the bit line of a non-selected memory cell are both applied with the ground voltage.

[c11] 11. The nonvolatile memory cell of claim 6, wherein when an erasing process is operated, the bit line and the word line are set to be floating or applied with a ground voltage, the first voltage terminal is applied with an erasing voltage, and the second voltage terminal is applied with the ground voltage.

[c12] 12. The nonvolatile memory cell of claim 11, wherein the word line and the bit line of a non-selected memory cell are both set to be floating or applied with the ground voltage.

[c13] 13. A structure of a non-volatile memory cell, comprising:
a first transistor, having a first source/drain (S/D) electrode coupled to a bit line, a gate electrode, and a second S/D electrode;
a second transistor, having a first source/drain (S/D) electrode coupled to a first voltage terminal, a gate electrode, and a second S/D electrode coupled to the second S/D electrode coupled of the first transistor; and
a shared capacitor structure, providing two capacitors

respectively coupled to the gate electrodes of the first transistor and the second transistor, wherein another electrode for each of the first transistor and the second transistor is coupled to a word line,
wherein the first transistor as a first cell and the second transistor as a second cell serve together as a dual-cell memory cell.

[c14] 14. The structure of the non-volatile memory cell of claim 13, wherein a failure occurs on the dual-cell memory cell only when the first cell and the second cell are both in failure function.

[c15] 15. The structure of the non-volatile memory cell of claim 13, further comprising a logic device.

[c16] 16. A nonvolatile memory cell, used for operation of multiple-time programming, comprising:
a plurality of sub-memory cells grouped as a memory cell, and adapted to a bit line and a word line, wherein the memory cell is programmed using the sub-memory cells one after one, so that the memory cell can be programmed for multiple times.

[c17] 17. The nonvolatile memory cell of claim 16, wherein the memory cell includes a shared capacitor structure.